WHAT IS CLAIMED IS:

1. A method for maintaining throughput in a data element, comprising the steps of:

receiving a clock and a plurality of instances of data having a first width on an input;

processing consecutive ones of the plurality of instances of data having the first width to produce more than one of a plurality of instances of data having a second width wherein the second data width are equivalent to the first data width and the more than one of the plurality of instances of data having the second data width are used to produce a plurality of instances of data having a third data width wherein the third data width are greater than the second data width and the plurality of instances of data having the third data width are used to produce a plurality of instances of data having an output data width wherein the output data width are equivalent to the third data width; and

transmitting the plurality of instances of data having the output data width.

2. The method according to claim 1, the processing step further comprising the steps of:

sampling consecutive ones of the plurality of instances of data having the first width at consecutive ones of a first rising edge and a falling edge of the clock;

generating more than one instance of a plurality of data having the second width;

converting the more than one instance of the plurality of data having the second width at a second rising edge of the clock to result in the plurality of instances of data having the third width data;

transmitting a handshake signal; and

transmitting the plurality of instances of data having the third data width.

3. The method according to claim 2, wherein the handshake signal is a pulse.

4. The method according to claim 2, wherein the first and second width data are 32 bits and the third and fourth width data are 64 bits.

5. The method as in claim 2, wherein the clock is received from a media independent interface.

6. The method according to claim 1 wherein the processing step includes a cyclic redundancy check (CRC).

7. The method according to claim 1 wherein the processing step includes statistics generation.

8. The method according to claim 1, wherein the processing step includes a dual data rate sampling.

9. The method according to claim 8 wherein the step of performing dual data rate sampling comprises the step of, sampling the plurality of instances of data having the first width on the input in accordance with a rising and falling edge of the clock to produce the more than one of the plurality of instances of data having the second width.

10. The method according to claim 9 wherein the first and second width data are 32 bits and the third and fourth width data are 64 bits.

11. The method according to claim 1 wherein the processing step comprises the step of resolving an inter-packet gap.

12. The method according to claim 1 wherein the processing step comprises the step of resolving a preamble detection.

13. The method according to claim 1 wherein the processing step comprises the step of resolving a data alignment.

14. The method according to claim 1 wherein the processing step comprises the step of resolving statistics.

15. The method according to claim 2 wherein the step of transmitting of the plurality of instances of data having the third data width is done after the step of transmitting the handshake signal.

16. The method according to claim 15, wherein the handshake is generated by a first-in-first-out element.

17. A method for maintaining throughput in a data element, comprising the steps of:

receiving at a first element a clock and a first plurality of instances of data having a first bit-width as an input;

transmitting the clock and first plurality of instances of data having the first width to a second element;

operating on the first plurality of instances of data having the first width to produce a second plurality of instances of data having a second width;

transmitting the clock and second plurality of instances of data having the second width to a third element;

operating on the second plurality of instances of data

having the second width to produce a third plurality of instances of data having a third width;

transmitting the third plurality of instances of data having the third width to a fourth element; and

operating on the third plurality of instances of data having the third width to produce a fourth plurality of instances of data having a fourth width.

18. The method according to claim 17,wherein the first width is 68.

19. The method according to claim 17, wherein the second width is 32.

20. The method according to claim 17, wherein the third width is 64.

21. The method according to claim 17, wherein the fourth width is 64.

22. The method according to claim 17, wherein the third and fourth widths are equal.

23. The method according to claim 17, further comprising the steps of:

receiving the fourth plurality of instances of data having the fourth width by a fifth element; and

transmitting a fifth plurality of instances of data having a fifth width which is half of the fourth width.

24. The method according to claim 17, wherein the first element is a physical layer device.

25. The method according to claim 17, wherein the second element is a management control element.

26. The method according to claim 17, wherein the third element is a receive function element.

27. The method according to claim 23, wherein the fourth element is a receive control element.

28. The method according to claim 23, wherein the fifth element is a system interface.

29. A switch having one or more switching modules that are capable of maintaining data throughput, comprising:

one or more ports for receiving a plurality of inbound packets and for transmitting a plurality of outbound packets;

a physical layer device coupled to the input ports for receiving the plurality of inbound packets;

a media independent interface coupled to the physical layer device for receiving the plurality of inbound packets from the physical layer device;

a media access controller coupled to the media independent interface for receiving the output of the media independent interface and for processing the output of the media independent interface to increase bit width; and

a packet switching controller coupled to the media access controller for receiving the increased bit width data and for transmitting the increased bit width data.

30. The switch according to claim 29, wherein the media access controller comprises:

a management control element coupled to the media

independent interface for receiving the output of the media independent interface and for stripping off control bits;

a receive function element coupled to the management control element for receiving the output of the management control element and for increasing the bit width of the output from the management control element; and

a receive control element coupled to the receive function element for receiving the increased bit width data from the receive function element and for transmitting the increased bit width data to the packet switching controller.

31. The switch according to claim 29, wherein the media access controller further comprises:

a transmit control element coupled to the packet switching controller for receiving the output of the packet switching controller; and

a transmit function element for receiving the output of the transmit control element and for operating on the output of the transmit control element.

32. The switch according to claim 30, wherein the management control element processes management control bits in its received data to retrieve status information from ISO layers below a MAC layer.

33. The switch according to claim 30, wherein the receive function element comprises a first and second gate element blocks, the first and secondgate element blocks receiving the plurality of inbound packets , and wherein said first and second gate element blocks sample said plurality of inbound packets on the leading and trailing edge of the clock, respectively, to generate more than one plurality of instances of data.

34. The switch according to claim 33, wherein said first and second gate element blocks output more than one plurality of instances of data and a third gate element block outputs a the increased bit width data wherein said third gate element block combines said more than one plurality of instances of data in accordance with a second rising edge of the clock.

35. The switch according to claim 34 wherein the receive function element further comprises a logic block coupled to the third gate element block for generating statistics, performing data alignment and performing cyclical redundancy checks on data output by the third gate element block.

36. The switch according to claim 30, wherein a first-in-first-out (FIFO) element is coupled to the receive control element.

37. A media access controller, comprising:

a first gate for sampling an input data stream having a first bit width in accordance with a first rising edge of a clock;

a second gate for sampling said input data stream in accordance with a first falling edge of a clock; and

a third gate coupled to said first and second gates for combining outputs of said first and second gates in accordance with a second rising edge of said clock to produce an output data stream having a second bit width greater than said first bit width.

38. The media access controller according to claim 37 further comprising a management control element for processing

management control bits in the input data stream to retrieve status information from ISO layers below a MAC layer.

39. The media access controller according to claim 37 further comprising a receive control element coupled to said third gate for providing flow control functionality.

40. The media access controller according to claim 37 further comprising a logic block coupled to the third gate for generating statistics.

41. A media access controller, comprising:

a first data path having a first bit-width; and

a second data path including a receive function element that receives input data at said first bit width and processes said input data to generate output data having a second bit width greater than said first bit width.

42. The media access controller according to claim 41 wherein said receive function element comprises:

a first gate for sampling said input in accordance with a first rising edge of a clock;

a second gate for sampling said input in accordance with a first falling edge of a clock; and

a third gate coupled to said first and second gates for combining outputs of said first and second gates in accordance with a second rising edge of said clock to produce said output data having said second bit width greater than said first bit width.

43. The media access controller according to claim 41 further comprising a management control element for processing

management control bits in the input data to retrieve status information from ISO layers below a MAC layer.

44. The media access controller according to claim 42 further comprising a receive control element coupled to said third gate for providing flow control functionality.

45. The media access controller according to claim 42 further comprising a logic block coupled to the third gate for generating statistics.

46. A method for maintaining throughput in a data element, comprising the steps of:

receiving a first data having first bit-width bits, management bits and clock bits; inputting the first bit-width bits and clock bits into a receive data path; and

processing the first bit-width bits to generate processed data having a second bit-width which is greater than said first bit-width.

47. The method according to claim 46 wherein the processing step further comprises:

receiving a clock having a clock rate; and

performing dual data rate sampling on the first bit width data in accordance with said clock to produce the processed data having a second bit-width which is greater than the first bit-width.

48. The method as in claim 47 wherein the step of performing dual data rate sampling on the receive data comprises sampling a first data stream in accordance with a rising and falling edge of the clock.

49. The method as in claim 47, wherein the clock is received from a media independent interface.

50. The method as in claim 47, wherein the step of performing dual data rate sampling on the first bit-width bits comprises inputting the first bit-width bits to two gates, one gate triggering on a rising edge of the clock and the other gate triggering on a falling edge of the clock.